sbRIO-based Multi-Sensor Excitation Low Voltage Chassis for Hall B Magnets

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Progress on the development of a new Multi-Sensor Excitation Low Voltage (MSELV) chassis for the Hall B magnets is presented in this note. This new chassis is based on National Instruments' (NI) single-board cRIO (sbRIO) controller. The improved chassis will eliminate a point of failure in the readout chain and provide new features for the readout system, made available by the sbRIO.

Hall B torus and solenoid use eight custom-built MSELV chassis to read out load cells, strain gauges, temperature sensors, and Hall-Effect sensors. The chassis in use have a DE0-Nano board instrumented with an Altera Cyclone IV FPGA and connect to a NI Compact-RIO (cRIO) to read out sensor data and communicate with the magnets' PLC [1].

Figure 1(a) shows the present readout chain. The DE0-Nano FPGA forwards sensor data to the LV cRIO, which has been a point of failure in the past; the plan is to eliminate this readout element using the new MSELV chassis, Fig. 1(b).

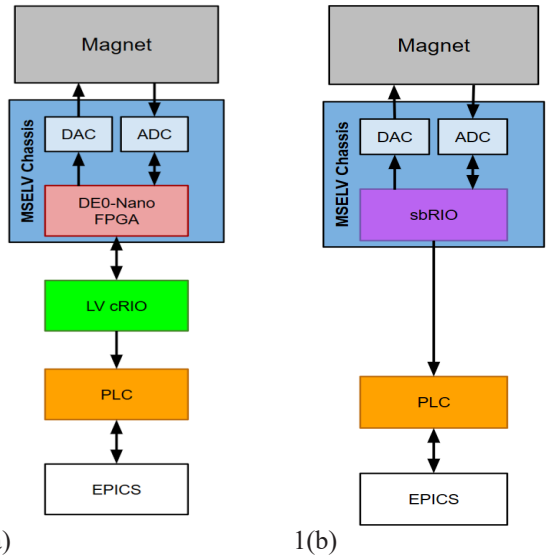

FIG. 1(a). Present MSELV chassis' data communication path. 1(b). Proposed sbRIO-based MSELV chassis data communication path.

To eliminate the LV cRIO, initial investigation and development used a DE0-Nano-System-on-a-Chip (SoC) board instrumented with a Cyclone V FPGA. However, the Cyclone V FPGA did not perform as advertised and the chip's internal FPGA – Hard Processing System bridging did not work as expected. Hence, an sbRIO was procured to investigate whether it could replace the Cyclone series FPGA in the MSELV chassis.

The procured sbRIO has a Xilinx Zynq-7000 SoC that can be programmed through LabVIEW as an FPGA and/or Real-Time device. Because the sbRIO has the same architecture as the current LV cRIO, the LV cRIO's program, in principle, should be able to run on the sbRIO.

Within the MSELV chassis, there are eight digital-to-analog converters (DACs) and four analog-to-digital converters (ADC). DACs set the excitation values for each sensor; ADCs read the resulting sense voltage from sensors. Table I contains the specifications of the DACs and ADCs used.

Device	Specification	Value
DAC	model	DAC8568ICPW
	number of channels	8
	resolution	16-bits (1 LSB = ~75 µV)
	output range	0 V–5 V
ADC	model	ADS1258IRTCT
	number of channels	16
	resolution	24-bits (1 LSB = ~300 nV)
	input range	0 V–2.5 V

TABLE I. MSELV chassis DAC and ADC specifications.

To communicate with the DACs and ADCs, subVIs were developed for the sbRIO's FPGA to generate necessary data input/output, clocking, and synchronization. Once these FPGA subVIs were developed, Real-Time subVIs could be developed to allow more complex calculations and communications to external devices. This allows the LV cRIO, Fig.1(a), to be eliminated. At this point, a basic working sbRIO-based MSELV chassis (MSELV-sbRIO) prototype has been completed.

Initial tests with fixed-resistance dummy loads show that the MSELV-sbRIO behaves as expected and provides the sensor measurements identical to the original MSELV chassis.

In summary, a prototype sbRIO-based MSELV chassis has been successfully developed and tested with fixed-resistance dummy loads. Future research and development efforts will focus on adding features that will improve the MSELV-sbRIO's flexibility in operation, allow sensor configuration to be changed while installed in the field, and act as its own device instead of relying on an external master controller.

[1] P. Bonneau, et al. *FPGA Upgrade Proposals for the Hall B Torus and Solenoid Control and Monitoring Systems*, DSG Note 2019-37, 2019.